CLAIMS:

1. A radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor, said power amplifier comprising:

(a) a circuit means for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier; and,

(b) a detector circuit means for detecting RF input to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

2. The linear power amplifier as claimed in Claim 1, wherein said circuit means for generating a bias signal producing a quiescent current comprises a differential transistor pair, said detector circuit means output signal being coupled directly to one side of said differential pair.

3. The linear power amplifier as claimed in Claim 2, further including a sliding bias circuit connected to another side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

4. The linear power amplifier as claimed in Claim 3, wherein the sliding bias circuit means includes means for automatically reducing the quiescent current for an output stage amplifier at power ranges below a certain power output threshold.

5. The linear power amplifier as claimed in Claim 1, comprising first and second power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage, for reducing said quiescent current at a second output stage.

6. The linear power amplifier as claimed in Claim 1, further comprising means for further modifying said quiescent current at a second output stage under discrete voltage control.

7. A communications device including a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor, said power amplifier comprising:

(a) a circuit means for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier;

(b) a detector circuit means for detecting RF input to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

8. The communications device as claimed in Claim 7, wherein said circuit means for generating a bias signal producing a quiescent current comprises a differential transistor pair, said detector circuit means output signal being coupled directly to one side of said differential pair.

9. The communications device as claimed in Claim 7, further including a sliding bias circuit connected to another side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

10. The communications device as claimed in Claim 7, further comprising means for further modifying said quiescent current at a second output stage under discrete voltage control.

11. A sliding bias circuit for dynamically controlling quiescent current flowing through an output transistor of a linear power amplifier operating in an output frequency band, said linear power amplifier comprising a circuit means for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said sliding bias circuit comprising:

a detector circuit means for detecting RF input to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said

quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

12. The sliding bias circuit as claimed in Claim 11, wherein said circuit means for generating a bias signal producing a quiescent current comprises a differential transistor pair, said detector circuit means output signal being coupled directly to one side of said differential pair.

13. The sliding bias circuit as claimed in Claim 11, wherein said linear power amplifier comprises first and second power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage, for reducing said quiescent current at a second output stage.

14. The sliding bias circuit as claimed in Claim 13, wherein said second power output stage further includes means for further modifying said quiescent current at a second output stage under discrete voltage control.